PCN
Product/Process Change Notification

Additional assembly and test line qualification for FERD diodes housed in DPAK package

Notification number:	ADG-DIS/18/10745	**Issue Date**	19/02/2018
Issued by	Aline AUGIS		
Product series affected by the change		FERDxxxSB-TR	
Type of change		Back-end realization	

Description of the change

Qualification of an additional back-end subcontractor located in China (location B) for the assembly and test and finishing of FERD products in DPAK as a double sourcing of location A (China).
Location B is already a major production site for ST, including Power Schottky and ultrafast diodes technologies.

Reason for change

STMicroelectronics investment on FERD capacity increase.

Former versus changed product:	The changed products do not present modified electrical, dimensional or thermal parameters, leaving unchanged the current information published in the product datasheet. The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged. The footprint recommended by ST remains the same. There is no change in the packing modes and the standard delivery quantities either. The products remain in full compliance with the ST ECOPACK®2 grade (“halogen-free”).

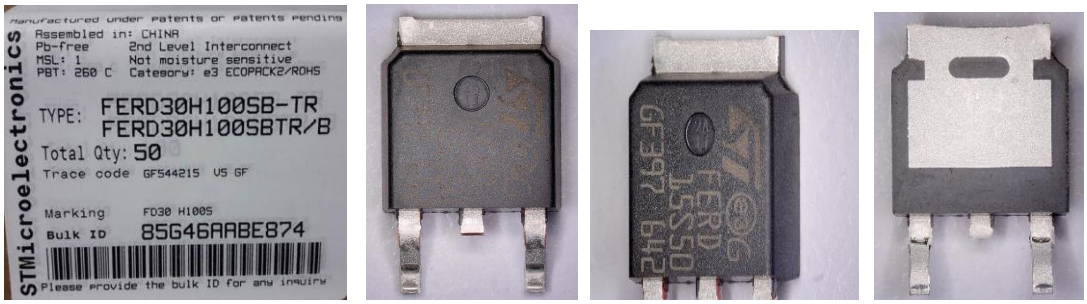
Disposition of former products

The current production will still run.
Shipments will be done from both former and new assembly locations.

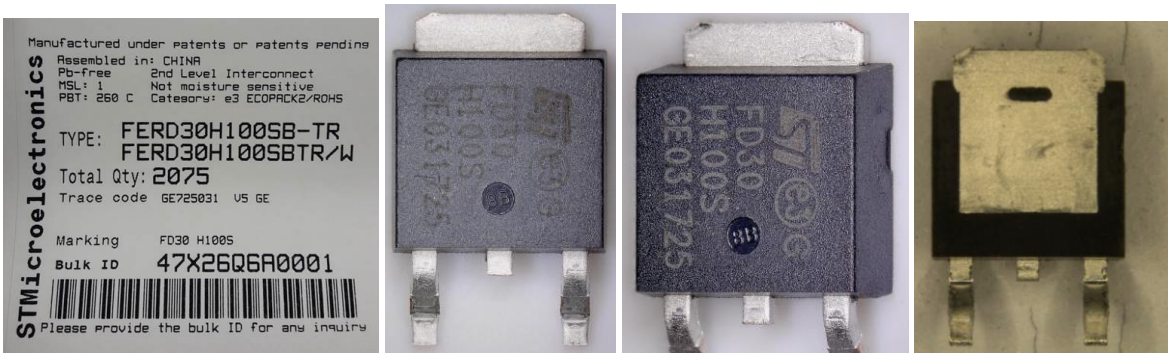
Marking and traceability:

The die marking is the same between plant A and B. Traceability of the BE plant will be ensured by an internal codification (Finished Good) and by trace code (die marking and on the carton box label). The first two digits of the trace code indicate the back end plant provenance.

LOCATION A



LOCATION B



Commercial Product	LOCATION A Finished Good	LOCATION B Finished Good	MARKING
FERD15S50SB-TR	FERD15S50SBTR/B	FERD15S50SBTR/W	FERD 15S50
FERD20H100SB-TR	FERD20H100SBTR/B	FERD20H100SBTR/W	FD20 H100S
FERD20S100SB-TR	FERD20S100SBTR/B	FERD20S100SBTR/W	FD20 S100S
FERD30H100SB-TR	FERD30H100SBTR/B	FERD30H100SBTR/W	FD30 H100S

Qualification complete date	**Week 48/2017**

Forecasted sample availability

Product family	Sub-family	Commercial part Number	Availability date
Rectifiers	DPAK	FERD15S50SB-TR	W05/2018
Rectifiers	DPAK	FERD20H100SB-TR	W05/2018
Rectifiers	DPAK	FERD20S100SB-TR	W05/2018
Rectifiers	DPAK	FERD30H100SB-TR	W05/2018

Change implementation schedule

Sales types	Estimated production start	Estimated first shipments
FERDxxxSB-TR	Week 51/2017	Week 21/2018

Comments:	

Customer's feedback

Please contact your local ST sales representative or quality contact for requests concerning this change notification.
Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change
Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change

Qualification program and results	17105QRP Attached

Reliability Evaluation Report

Qualification of FERDxxxSB-TR at additional subcontractor in China 994X

General Information	
Product Line	*RECTIFIERS*
Product Description	*AFER diode*
Product	*FERD15S50SB-TR* *FERD20H100SB-TR* *FERD20S100SB-TR* *FERD30H100SB-TR*
Product Group	*ADG*
Product division	*ASD&IPAD*
Package	*DPAK*
Maturity level step	*Qualified*

Locations	
Wafer fab	*ST Catania (ITALY)*
Electrical Wafer Sorting	*ST SINGAPORE*
Assembly plant	Subcontractor 994X (CHINA)
Reliability Lab	*ST Tours (FRANCE)*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
0.1	19-Oct-2017	7	Isabelle BALLON	Julien MICHELON	Initial release

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices

2 GLOSSARY

SS	Sample Size
PC	Pre-conditioning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
THB	Thermal Humidity Bias
UHAST	Unbiased Highly Accelerated Stress Test
SD	Solderability
RSH	Resistance to Soldering Heat
DBT	Dead Bug Test
GD	Generic Data

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify Field-Effect Rectifier Diodes, FERDxxxSB-TR mounted in DPAK package at additional subcontractor in China (994X).

Product	Package	Assembly location
FERD15S50SB-TR FERD20H100SB-TR FERD20S100SB-TR FERD30H100SB-TR	DPAK	Subcontractor 994X (China)

The reliability test methodology used follows the JESD47: « Stress Test Driven Qualification Methodology » guidelines. The following reliability tests ensuing are:

- TC to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- THB, UHAST to check the robustness to corrosion and the good package hermeticity.
- RSH, Solderability and DBT to check compatibility of package with customer assembly.

The qualification plan is based on similarity methodology. See 5.1 “comments” for more details.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Devices description

Refer products datasheets.

4.2 Construction note

See referenced Product Baseline for detailed information.

	FERDxxxSB-TR
Wafer/Die fab. information	
Wafer fab manufacturing location	ST CATANIA – ITALY
Technology / Process family	AFER
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST SINGAPORE
Assembly information	
Assembly site	Subcontractor 994X (China)
Package description	DPAK
Molding compound	ECOPACK® molding compound
Lead finishing material	Tin (Sn)
Final testing information	
Testing location	Subcontractor 994X (China)

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Test vehicles for FERDxxxSB-TR				
Lot #	**Commercial product**	**Package**	**Assy / Test location**	**Comments**
L1	FERD30H100SB-TR	DPAK	Subcontractor 994X (China)	Similar die technology (Larger die) with higher voltage

Detailed results in below chapter will refer to P/N and Lot #.

5.2 Test plan and results summary

FERDxxxSB-TR qualification test plan and results						
Test	**PC ****	**Std ref.**	**Conditions**	**Steps / Duration**	**SS**	**Failure/SS**
						L1
Die oriented Tests						
HTRB	N	JESD22 A-108	VR=0.8xVrrm Ta=(*)	1Khrs	77	0/77
Package oriented Tests						
TC	Y	JESD22 A-104	-65/+150°C 2cy/h	500cy	77	0/77
THB	Y	JESD22 A-101	85°C; 85% RH VR=0.8xVRRM (limited to 100V)	1Khrs	77	0/77
UHAST	Y	JESD22 A-118	130°C 85% RH	96hrs	77	0/77
SD	Y	JESD22 B-102	Dry ageing SnPb bath 220°C	-	10	0/10
			Wet ageing SnPb bath 220°C	-	10	0/10
			Dry ageing SnAgCu bath 245°C	-	10	0/10
			Wet ageing SnAgCu bath 245°C	-	10	0/10
RSH	Y	JESD22 A-111	85°C/85%RH Ageing 168hrs 10sec solder dipping 260°C	-	-	Not applicable acc. JESD22A-111 vs package/die paddle size
DBT	Y	DM00112629 (ST internal)	IR reflow after flux deposition	-	30	0/30

Note: Whiskers positive data available from monitoring only.

* Maximal available temperature preventing from thermal runaway corresponding to Ta =120°C, Tj~125°C

** All package-oriented tests are submitted to preconditioning PC before test.

6 ANNEXES

6.1 Tests Description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
UHAST Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
SD Solderability	Wet/Dry ageing + dipping in a solder bath. Assessment by visual inspection of the leads.	To check package ability to be soldered with no difficulty. To simulate whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly at customer using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.
RSH Resistance to Soldering Heat	Package is dipped by the leads in a solder bath after an initial wet ageing.	To simulate wave soldering process and verify that package will not be thermally damaged during this step.
DBT Dead Bug Test	Leads are covered with soldering flux and are submitted to IR reflow. Assessment by visual inspection of the leads	To ensure good wettability of the leads